**CIS 350 – INFRASTRUCTURE TECHNOLOGIES**

**GROUP HOMEWORK #5, PART I**

**Topics: Machine Cycle, Registers, and Memory (Chapter 7)**

Group # and Names of Group Members:

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Logistics

1. Get in touch with your group. (See Groups folder on Blackboard.)
2. Discuss and work all 3 problems collectively with your group via E-mail, Discussion Forum, Blackboard Collaborate Ultra, and/or MS Teams. (Do not divide the work among group members.)
3. Choose a recorder to prepare the final copy (**one per group**) and submit it via the Blackboard Assignments/Homeworks folder by the due date.
4. Be sure all group members' names are on final copy. Do **not** add names of your group members who did not participate in the assignment or whose contribution was minimal.

Worth 60 points.

**Problem 1**. Suppose that the following instruction is found at the given address/location in memory:

Address Instruction

05 LDA 20

06 ….

…. Data

20 15

The instruction LDA 20 residing at address 05 loads the contents of memory location 20, which is 15, into the Accumulator (A).

(a) Draw the diagram below showing the flow and contents of the CPU (PC, IR, A), MAR, Memory, and MDR, after each of the 5 steps of the fetch-execute cycle is executed. Number the steps 1-5. For help see page 5 in the lecture notes for Chapter 7 and the video recording of Chapter 7.

A diagram of a flowchart

Description automatically generated

(b) Fill in the table below with the contents of the PC, MAR, MDR, IR, and A as each of the 5 steps of the fetch-execute cycle is performed for that instruction. If the content of the register is unknown, write a question mark "?".

PC MAR MDR IR A

(1) PC → MAR \_\_05\_\_ \_\_05\_\_ \_\_LDA 20\_\_ \_\_?\_\_ \_\_?\_\_

(2) MDR → IR \_\_05\_\_ \_\_05\_\_ \_\_LDA 20\_\_ \_\_LDA 20\_\_ \_\_?\_\_

(3) IR [address] → MAR \_\_05\_\_ \_\_20\_\_ \_\_15\_\_ \_\_LDA 20\_\_ \_\_?\_\_

(4) MDR → A \_\_05\_\_ \_\_20\_\_ \_\_15\_\_ \_\_LDA 20\_\_ \_\_15\_\_

(5) PC+1 → PC \_\_06\_\_ \_\_20\_\_ \_\_15\_\_ \_\_LDA 20\_\_ \_\_15\_\_

**Problem 2**. Suppose that the following instructions are found at memory locations 01 and 02. Suppose that the following data are found at memory 15 and 16.

Address Instruction

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01 LDA 15

02 SUB 16 Addresses 01-02 represent the program area

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Data

15 20 Addresses 15-16 represent the data area

16 6

Show the contents of the PC, MAR, MDR, IR, and A registers as each step of the fetch-execute cycle is performed for instructions at addresses 01 and 02. Note that you have a sequence of two instructions. The 5 steps in the second instruction SUB 16 will gradually replace the contents of the registers set by the first instruction.

The machine cycle for the LDA instruction that is in the lecture notes for Chapter 7 and that we discussed on Panopto and/or MS Teams would be helpful.

Instruction: 01 LDA 15

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Steps in the machine cycle | PC | MAR | MDR | IR | A |
| 1. PC → MAR | 1 | 1 | LDA 15 | ? | ? |
| 2. MDR → IR | 1 | 1 | LDA 15 | LDA 15 | ? |
| 3. IR[addr] → MAR | 1 | 15 | 20 | LDA 15 | ? |
| 4. MDR → A | 1 | 15 | 20 | LDA 15 | 20 |
| 5. PC + 1 → PC | 2 | 15 | 20 | LDA 15 | 20 |

Instruction: 02 SUB 16

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Steps in the machine cycle | PC | MAR | MDR | IR | A |
| 1. PC → MAR | 2 | 2 | SUB 16 | LDA 15 | 20 |
| 2. MDR → IR | 2 | 2 | SUB 16 | SUB 16 | 20 |
| 3. IR[addr] → MAR | 2 | 16 | 6 | SUB 16 | 20 |
| 4. A - MDR → A | 2 | 16 | 6 | SUB 16 | 14 |
| 5. PC + 1 → PC | 3 | 16 | 6 | SUB 16 | 14 |

**Problem 3**

1. The following sequence of steps in the instruction cycle

PC → MAR

MDR → IR

If A=0 Then IR [address] → PC Else PC+1 → PC What instruction does it represent? \_\_\_BRZ\_\_\_\_

**The possibilities are: LDA, STO, SUB, ADD, IN, OUT, HLT, BR, BRP, and BRZ.**

2. The following sequence of steps in the instruction cycle

PC → MAR

MDR → IR

If A≥0 Then IR [address] → PC Else PC+1 → PC What instruction does it represent? \_\_\_BRP\_\_\_\_

3. The following sequence of steps in the instruction cycle

PC → MAR

MDR → IR

In-basket → A

PC + 1 → PC What instruction does it represent? \_\_\_IN\_\_\_

4. The following sequence of steps in the instruction cycle

PC → MAR

MDR → IR

IR [address] → MAR

A + MDR → A

PC+1 → PC What instruction does it represent? \_\_\_ADD\_\_\_

5. The following sequence of steps in the instruction cycle

PC → MAR

MDR → IR

IR [address] → PC What instruction does it represent? \_\_\_BR\_\_\_\_

6. The following sequence of steps in the instruction cycle

PC → MAR

MDR → IR

IR [address] → MAR

A - MDR → A

PC+1 → PC What instruction does it represent? \_\_\_SUB\_\_\_

7. The following sequence of steps in the instruction cycle:

PC → MAR

MDR → IR

IR [address] → MAR

MDR → A

PC+1 → PC What instruction does it represent? \_\_\_LDA\_\_\_

8. The following sequence of steps in the instruction cycle

PC → MAR

MDR → IR

PC → 0 or PC → PC (remains the same) What instruction does it represent? \_\_\_HLT\_\_\_

9. The following sequence of steps in the instruction cycle

PC → MAR

MDR → IR

A → Out-basket

PC + 1 → PC What instruction does it represent? \_\_\_OUT\_\_\_

10. The following sequence of steps in the instruction cycle:

PC → MAR

MDR → IR

IR [address] → MAR

A → MDR

PC+1 → PC What instruction does it represent? \_\_\_STO\_\_\_